In the claims

Please amend the claims as follows:

1. (Currently Amended) A variable gain amplifier, comprising:

an input signal provision and variable gain controller for receiving first and second input signals via a differential pair of a cascode input shape and amplifying a difference signal of the first and second input signals to output first and second differential signals, wherein the controller controls a variable voltage gain of the difference signal according to a gain control voltage signal; and

a current/voltage converter for receiving the first and second differential signals outputted from the input signal provision and variable gain controller and converting the first and second differential signals into first and second output voltages of a voltage inputted type depending on first and second bias voltages,

wherein the input signal provision and variable gain controller is under ~~the negative feedback~~ a negative feedback from the current/voltage converter and thus has the construction of a current inputted type or the voltage inputted type.

2. (Original) The variable gain amplifier as claimed in claim 1, wherein the input signal provision and variable gain controller comprises:

a first NMOS transistor having a source terminal connected to a first node of the current/voltage converter and a gate terminal to which the first input signal is inputted;

a second NMOS transistor constituting a differential type together with the first NMOS transistor, and having a source terminal connected to a second node of the current/voltage converter and a gate terminal to which the second input signal is inputted;

a third NMOS transistor having a source terminal connected to a drain terminal of the first NMOS transistor and a drain terminal connected to a third node of the

current/voltage converter, and driven by the gain control voltage signal; and

a fourth NMOS transistor having a source terminal connected to a drain terminal of the second NMOS transistor and a drain terminal connected to a fourth node of the current/voltage converter, and driven by the gain control voltage signal.

3. (Original) The variable gain amplifier as claimed in claim 2, wherein the first and third NMOS transistors and the second and fourth NMOS transistors operate in a saturation region or a triode region depending on the gain control voltage signal.

4. (Original) The variable gain amplifier as claimed in claim 1, wherein the input signal provision and variable gain controller comprises:

a first NMOS transistor having a source terminal connected to a fifth node of the current/voltage converter and a gate terminal to which the first input signal is inputted;

a second NMOS transistor forming a differential type along with the first NMOS transistor, and having a source terminal connected to the fifth node of the current/voltage converter and a gate terminal to which the second input signal is inputted;

a third NMOS transistor having a source terminal connected to a drain terminal of the first NMOS transistor and a drain terminal connected to a third node of the current/voltage converter, and driven by the gain control voltage signal; and

a fourth NMOS transistor having a source terminal connected to a drain terminal of the second NMOS transistor and a drain terminal connected to a fourth node of the current/voltage converter, and driven by the gain control voltage signal.

5. (Original) The variable gain amplifier as claimed in claim 4, wherein the first and third NMOS transistors, and the second and fourth NMOS transistors operate in a saturation region or a triode region according to the gain control voltage

signal.

6. (Original) The variable gain amplifier as claimed in claim 1, wherein the current/voltage converter comprises:

a first resistor connected between a power supply voltage source and a first node to which the first differential signal is inputted;

a second resistor connected between the power supply voltage source and a second node to which the second differential signal is inputted; and

a DC bias means connected between the first and second resistors and the ground voltage source and operating as a current source according to the first and second bias voltage, for providing a DC bias of the first and second output voltages outputted from the current/voltage converter.

7. (Currently Amended) The variable gain amplifier as claimed in claim 6, wherein the DC bias means comprises:

a first NMOS transistor connected between the first node and a ~~third~~ fourth node for negative feedback of a first current to the input signal provision and variable gain controller, and driven by the first bias voltage;

a second NMOS transistor connected between the second node and a ~~fourth~~ third node for negative feedback of a second current to the input signal provision and variable gain controller, and driven by the first bias voltage;

a third NMOS transistor connected between ~~a~~ the third node and the ground voltage source and driven by the second bias voltage; and

a fourth NMOS transistor connected between ~~a~~ the fourth node and the ground voltage source and driven by the second bias voltage.

8. (Currently Amended) The variable gain amplifier as claimed in claim 6, wherein the DC bias means comprises:

a first NMOS transistor connected between the first node and a fourth ~~third~~

node for negative feedback of a voltage to the input signal provision and variable gain controller, and driven by the first bias voltage;

a second NMOS transistor connected between the second node and the third node and driven by the first bias voltage;

a third NMOS transistor connected between the third node and the ground voltage source and driven by the second bias voltage; and

a fourth NMOS transistor connected between the ~~third~~ fourth node and the ground voltage source and driven by the second bias voltage.

9. (Original) The variable gain amplifier as claimed in claim 1, wherein the current/voltage converter comprises:

a first active load circuit connected between a power supply voltage source and a first node to which the first differential signal is inputted;

a second active load circuit connected between the power supply voltage source and a second node to which the second differential signal is inputted; and

a DC bias means connected between the first and second active load circuits and a ground voltage source, and driven as a current source according to the first and second bias voltages, for providing a DC bias of the first and second output voltages outputted from the current/voltage converter.

10. (Original) The variable gain amplifier as claimed in claim 9, wherein the first active load circuit comprises:

a first PMOS transistor connected between the power supply voltage source and the first node and driven by the potential of a third node;

a first NMOS transistor constituting a reciprocal negative feedback along with the first PMOS transistor, connected between the supply voltage source and the third node, and driven by the potential of the first node;

a first current source connected between the third node and the ground voltage source, for providing a bias current of the first active load circuit; and

a frequency compensation capacitor connected between the third node and the ground voltage source, for improving a frequency characteristic of the first active load circuit.

11. (Original) The variable gain amplifier as claimed in claim 9, wherein the second active load circuit comprises:

a first PMOS transistor connected between the supply voltage source and the second node and driven by the potential of a third node;

a first NMOS transistor constituting a reciprocal negative feedback along with the first PMOS transistor, connected between the power supply voltage source and the third node, and driven by the potential of the second node;

a first current source connected between the third node and the ground voltage source, for providing a bias current of the second active load circuit; and

a frequency compensation capacitor connected between the third node and the ground voltage source, for improving a frequency characteristic of the second active load circuit.

12. (Currently Amended) The variable gain amplifier as claimed in claim 9, wherein the DC bias means comprises:

a first NMOS transistor connected between the first node and a ~~third~~ fourth node for negative feedback of a first current to the input signal provision and variable gain controller, and driven by the first bias voltage;

a second NMOS transistor connected between the second node and a ~~fourth~~ third node for negative feedback of a second current to the input signal provision and variable gain controller, and driven by the first bias voltage;

a third NMOS transistor connected between the third node and the ground voltage source and driven by the second bias voltage; and

a fourth NMOS transistor connected between the fourth node and the ground voltage source and driven by the second bias voltage.

13. (Currently Amended) The variable gain amplifier as claimed in claim 9, wherein the DC bias means comprises:

a first NMOS transistor connected between the first node and a ~~third~~ fourth node for negative feedback of a voltage to the input signal provision and variable gain controller, and driven by the first bias voltage;

a second NMOS transistor connected between the second node and a third node and driven by the first bias voltage;

a third NMOS transistor connected between the third node and the ground voltage source and driven by the second bias voltage; and

a fourth second NMOS transistor connected between the ~~third~~ fourth node and the ground voltage source and driven by the second bias voltage.